



Design and Analysis of Phase Lock Loop Based Frequency Synthesizer Using Source Coupled Voltage Controlled Oscillator

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ABSTRACT

The Complementary Metal Oxide Semiconductor (CMOS) PLL based frequency synthesizer is a vital role in Receiver front end sub component. In general, the Phase Locked Loop (PLL) contains Phase Frequency Detector (PFD), Charge pump, Loop filter, Voltage controlled oscillator (VCO) and Frequency divider. Voltage controlled oscillator (VCO) is a critical building block in PLL which decides the power consumed by the PLL and area occupied by the PLL. Here the Source coupled VCO is proposed with adaptive voltage level technique to reduce the power consumption, then design of PLL and clock recovery circuit by using different types of VCO and results are compared between them it is designed in LTSPICE.

KEY WORDS: Harmonics, Frequency, Voltage Controlled Oscillator, Phase Lock Loop and Coupled Voltage.

1. INTRODUCTION:

A frequency synthesizer (FS) is a feedback system that generates one or many frequencies from one or a few frequency sources. The output of an FS is characterized by its frequency tuning range, frequency resolution, and frequency purity but some uncertainty of a synthesizer's output is characterized by its phase noise (or spur level) at a certain frequency offset from the desired carrier frequency in unit of dBc/Hz (or dBc). The

unit of dBc/Hz measures the ratio (in dB) of the phase noise power in 1Hz bandwidth at a certain frequency offset to the carrier power. Frequency synthesizers can be grouped into two classes: direct synthesis and indirect synthesis. Direct synthesis is classified in direct analog synthesizer (DAS) and direct digital synthesizer (DDS). Indirect synthesis is classified in phase-locked loop frequency synthesizer (PLL-FS), and delay-locked loop frequency synthesizer (DLL-FS). In this paper focused on PLL based frequency synthesizer. It is categories in integer-N and fractional-N synthesizer on the basis of programmable divider. Phase-locked loop is